WHAT IS CLAIMED IS:

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1. A semicustom integrated circuit comprising:
(a) a plurality of cell rows, in each row a plurality of standard cells are arranged; and
(b) gate array basic cells formed in an empty space of a predetermined cell row of the plurality of cell rows.

2. The integrated circuit of claim 1, wherein respective standard cells are formed on a basis of a rectangular pattern region having a predetermined height and a predetermined width, and the basic cells are formed on a basis of a rectangular pattern having a height substantially identical to that of the standard cells.

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3. The integrated circuit of claim 1, further comprising:
gate array basic cells formed in wiring channel regions disposed between the plurality of cell rows.

4. The integrated circuit of claim 1, wherein respective cell rows are arranged adjacently.

5. The integrated circuit of claim 3, wherein the basic cells formed in the wiring channel regions are formed on a basis of a rectangular pattern having a height substantially identical to that of the standard cells.

6. The integrated circuit of claim 3, wherein the standard cells and the basic cells are arranged adjacently along a direction orthogonal to the cell rows.

7. The integrated circuit of claim 4, wherein the standard cells and the basic cells are arranged adjacently along a direction orthogonal to the cell rows.

8. The integrated circuit of claim 3, wherein the

standard cells and the basic cells which are arranged adjacently along a direction orthogonal to the cell rows have common signal lines.

9. The integrated circuit of claim 4, wherein the standard cells and the basic cells which are arranged adjacently along a direction orthogonal to the cell rows have common signal lines.

10. The integrated circuit of claim ~~2~~ 1, wherein the standard cells and the basic cells have common power supply lines arranged along a straight line.

11. The integrated circuit of claim ~~2~~ 1, wherein the standard cells and the basic cells have common signal lines arranged along a straight line.

12. The integrated circuit of claim ~~2~~ 1, wherein widths of the standard cells are integral multiple of a width of the basic cells.

13. The integrated circuit of claim 5, wherein widths of the standard cells are integral multiple of a width of the basic cells.

14. The integrated circuit of claim 1, wherein the standard cells and the basic cells are arranged pursuant to a same grid system.

15. The integrated circuit of claim 3, wherein the standard cells and the basic cells are arranged pursuant to a same grid system.

16. The integrated circuit of claim 1, wherein the basic cells are used to construct intermediate buffers for distributing a clock signal to a plurality of circuits

which are displaced on a semiconductor substrate.

17. The integrated circuit of claim 3, wherein the basic cells are used to construct intermediate buffers for distributing a clock signal to a plurality of circuits which are displaced on a semiconductor substrate.

18. The integrated circuit of claim 1, wherein the basic cells are used to construct additional circuits for increasing driving capability to drive signals transmitted to a plurality of circuits disposed on a semiconductor substrate.

19. The integrated circuit of claim 3, wherein the basic cells are used to construct additional circuits for increasing driving capability to drive signals transmitted to a plurality of circuits disposed on a semiconductor substrate.

20. A semicustom integrated circuit having a logic circuit area and at least one of megacell and megafunction on a single semiconductor chip, the logic circuit area comprising:

(a) a plurality of cell rows, in each row a plurality of standard cells are arranged; and

(b) gate array basic cells formed in an empty space of the standard cells in predetermined cell row of the plurality of cell rows.

21. The integrated circuit of claim 20, wherein respective standard cells are formed on a basis of a rectangular pattern having a predetermined height and a predetermined width, and the basic cells are formed on a basis of a rectangular pattern having a height substantially identical to that of the standard cells.

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22. The integrated circuit of claim 20, further comprising:

gate array basic cells formed in wiring channel regions between the plurality of cell rows.

23. The integrated circuit of claim 20, wherein the standard cells and the basic cells are arranged pursuant to a same grid system.

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